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The performance analysis of an HVDC link

This paper presents the results of a simulation study on a 12-pulse HVDC (High Voltage Direct Current) using a system in Simulink, specialized Toolbox in Matlab for simulating control systems. The object of the study was to investigate the steady state and dynamic performance of the system. First, response of current regulator after change in current reference is examined in order to see the behaviour of the controllers in controlling the desired current. Next, the digital simulation of a test system is presented and the response to a DC fault in the line and the AC fault at inverter side is shown. The results are evaluated to enhance the recovery of the system from the disturbances and voltage dependent current limits (VDCOL) for a full range of typical system disturbances. The presented approach benefits from Simulink's advantages in modeling and simulating dynamical systems. The simulation results are compared with other studies using EMTP (Electromagnetic Transient Program) and EMTDC (Electromagnetic Transient Program DC Analysis).

1. INTRODUCTION

High voltage direct current (HVDC) converts AC voltage to DC voltage in a rectifier and transmits DC power through the transmission line, and then reconverts DC into AC power in inverter and supplies the power. As a voltage, current and transmission power in the DC transmission can be controlled rapidly, when compared with the AC transmission, it is robust against a disturbance and increases a dynamic characteristic of AC power system and decreases a short-circuit capacity. The controllability of HVDC links is often cited as an important advantage of DC systems. This controllability can be valuable in improving the dynamic performance of large power systems. To achieve the promised advantages, control systems must perform appropriately for various disturbances and system condition.

HVDC technology finds application in the transmission of power over long distances or by means of underwater cable, and in the interconnection of differently managed power systems which may be operated synchronously or asynchronously [1, 2].

Several general purpose mathematical modeling applications are now providing advanced environments for solving complex network problems. Matlab uses a specialized Toolbox, named

Simulink, for simulating control systems. Simulink is capable of simulating dynamical systems has a powerful graphic user-interface with a large library of blocks [1, 3, 4].

The work presented here uses an example of an HVDC link in order to simulate its steady and dynamic state operation. Perturbations which consist on AC-DC fault conditions are applied with the goal of examining system performance. Compared with other research tasks, the results are obtained accurately and efficiently by Simulink.

2. HVDC SYSTEM MODEL

The HVDC system modelled, using the Simulink package, is based on a point-to-point DC transmission system. The DC system is a monopolar, 12 pulse converter using two universal bridge connected in series, rated 1000 MW (2000 A, 500 kV) at the inverter. DC interconnection is used to transmit power from a 500 kV, 5000 MVA, 60 Hz network (system 1) to 345 kV, 10 000 MVA, 50 Hz network (system 2). The receiving end and sending end ac systems are separated by a 300 km transmission line (figure 1).

2.1. The AC system

The AC networks, both at the rectifier and inverter end, are modelled as infinite sources separated from their respective commutating buses by system impedances. The impedances are represented as L-R/L networks having the same damping at the fundamental and the third harmonic frequencies. The impedance angles of the receiving end and the sending end systems are selected to be 80 degrees. This is likely to be more representative in the case of resonance at low frequencies [5, 8, 9].

2.2. The Converter transformers

The 1200 MVA converter transformer is modelled with three-phase transformer (Three-Windings). The parameters adopted (based on AC rated conditions) are considered as typical for transformers found in HVDC installation such as leakage: X = 0.24 p.u.(per unit).

2.3. The DC side of the system

The DC side of the converter system consists of a smoothing reactor (0.5 H) for the rectifier and the inverter bridges. The DC line is modelled in distributed parameter line model with lumped losses. This model is based on the Bergeron's travelling wave method used by the Electromagnetic Transient Program (EMTP) for a more realistic simulation. In this model, the lossless distributed LC line is characterized by two values: the surge impedance Z_C and the phase velocity v.

The model uses the fact that the quantity ($e + Z_C i$), where e is line voltage and i is line current, entering one end of the line must arrive unchanged at the other end after a transport delay of $\tau = d/v$, where d is the line length. By lumping $R/4$ at both ends of the line and $R/2$ in middle and using the current injection method of the power system blockset, the two following port model is derived:

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$$I_{sh}(t) = \left(\frac{1+h}{2}\right)\left[\frac{1}{Z}e_r(t-\tau) + hi_r(t-\tau)\right] + \left(\frac{1-h}{2}\right)\left[\frac{1}{Z}e_s(t-\tau) + hi_s(t-\tau)\right],\qquad(1)$$

$$I_{rh}(t) = \left(\frac{1+h}{2}\right)\left[\frac{1}{Z}e_s(t-\tau) + hi_s(t-\tau)\right] + \left(\frac{1-h}{2}\right)\left[\frac{1}{Z}e_r(t-\tau) + hi_r(t-\tau)\right],\qquad(2)$$

where $I_{sh}(t)$ is the current source sending end, $I_{rh}(t)$ is the current source receiving end,

$h = (Z_C - R/4)/(Z_C + R/4)$, $Z = Z_C + R/4$.

2.4. AC filters and capacitor banks

On AC side of 12-pulse HVDC converter, current harmonics of the order of 11, 13, 25 and higher are generated. Filters are installed in order to limit the amount of harmonics to the level required by the network. In the conversion process the converter consumes reactive power which is compensated in part by the filter banks and the rest by capacitor banks of 600 MVAR on each side.
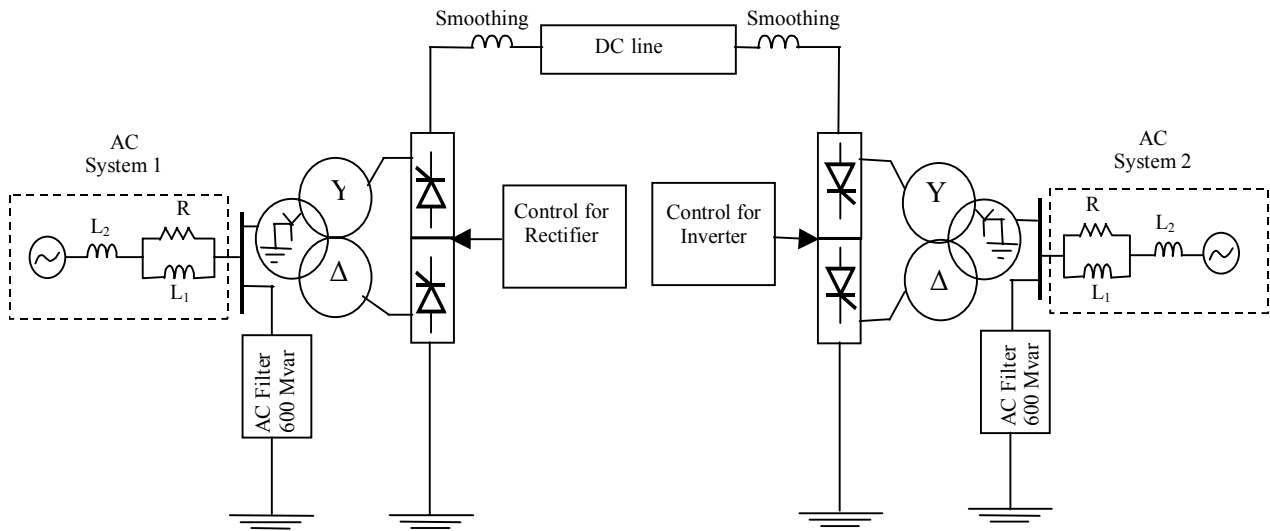

Fig. 1. HVDC system

3. CONTROL SYSTEMS

HVDC transmission systems must transport very large amounts of electric power that can only be accomplished under tightly controlled conditions. DC current and voltage is precisely controlled to affect the desired power transfer. It is necessary therefore to continuously and precisely measure system quantities that include at each converter bridge, the DC current, its DC side voltage and the delay angle α and for an inverter, its extinction angle γ [10, 11].

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3.1. Inverter control system

The inverter is in constant extinction angle (CEA) control. An error signal is derived from the difference between the reference γ and the measured γ. This error is fed through a PI controller to produce an α-order signal, which controls the firing pulses to the converter thyristors.

3.2. Rectifier control system

The DC link current is maintained by using a current controller at the rectifier. This controller performs its task by generating a control voltage, which then controls the firing pulses, at some delay angle α, to the rectifier valves. The relationship between DC current I_d and delay angle α is obtained by using the expression for the DC voltage at the rectifier, which is given by [2, 5]:

$$V_{dr} = V_{d0r} \cos(\alpha) - X_{cr} I_d ,$$ (3)

where V_{dr} is the DC line voltage, V_{d0r} is the open circuit rectifier DC voltage, X_{cr} is the equivalent reactance of rectifier.

For constant I_d, and small changes in α

$$\Delta V_{dr} / \Delta \alpha = V_{d0r} \sin(\alpha) .$$ (4)

The relationship between DC current and alpha is given by:

$$I_d = \frac{V_{d0r} \cos(\alpha) - V_{d0i} \cos(\gamma)}{R_{dc} + X_{cr} - X_{ci}} ,$$ (5)

where V_{d0i} is the open circuit inverter DC voltage, α is the rectifier firing (delay) angle, γ is the inverter extinction angle, R_{dc} is the DC line resistance, X_{ci} is the equivalent reactance of inverter.

The rectifier and inverter controls both have a voltage and a current regulator operating in parallel and calculating firing angles alpha. The effective angle is the minimum of these two angles. Both regulators are proportional and integral types with gains K_p and K_i.

Another particularity of the regulator is the linearization of the proportional gain. As V_d generated by the rectifier and the inverter is proportional to $\cos\alpha$ (eq. 3), the variation in V_d due to change in α is proportional to $\sin\alpha$ (eq. 2). With a constant K_p, the effective gain would therefore be proportional to $\sin\alpha$. In order to keep a constant proportional gain, independent of α, the gain is linearized by multiplying K_p with $(1/\sin\alpha)$. This linearization is applied for range of α defined by two limits ($5° < \alpha < 165°$ for rectifier, $92° < \alpha < 165°$ for inverter).

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3.3. The VDCOL function

In normal operation, the rectifier controls the current at the Id_ref reference value whereas the inverter controls the voltage at the Vd_ref reference value. The I_margin and Vd_margin parameters are respectively 0.1 p.u. and 0.05 p.u. The system normally operates at point 1 as shown in figure 2. However, during a severe contingency producing a voltage drop on the AC system 1 feeding the rectifier, the operating point will move to point 2. The rectifier will therefore be forced to α minimum mode and the inverter will be in current control mode.

Another important control function is implemented to change the reference current according to the value of the DC voltage. This control named Voltage Dependent Current Order Limits (VDCOL) automatically reduces the reference current (Id_ref) set point when VdL (Vd line) decreases (as for example, during a DC line fault or a severe AC fault). Reducing the Id reference currents also reduces the reactive power demand on AC network, helping to recover from fault [5]. The VDCOL parameters of the discrete 12-Pulse HVDC control are presented in figure 3.

The Id_ref value starts to decrease when the Vd line voltage falls bellow a threshold value VdThresh (0.6 p.u.). The actual reference current is named Id_ref-lim. IdMinAbs is the absolute minimum Id_ref set at 0.08 p.u. When the DC line voltage falls bellow the VdThresh value, the VDCOL reduces instantaneously Id_ref. However, when the DC voltage recovers, VDCOL limits the Id_ref rise time with a time constant [3, 8].
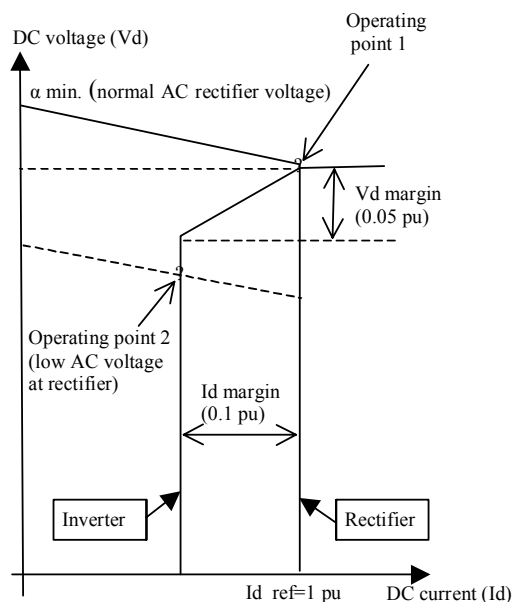

Fig. 2. Rectifier and inverter operating characteristic

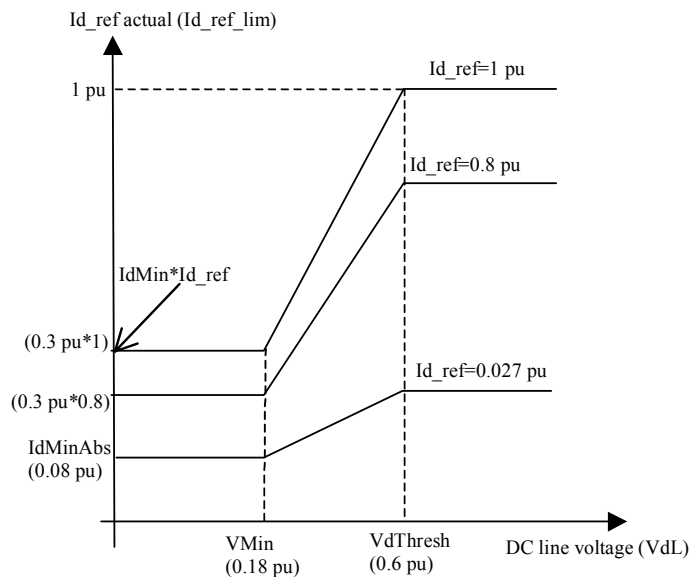Fig. 3. VDCOL characteristic

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4. SIMULATION RESULTS

The behaviour of the controllers in controlling the desired current for typical system disturbances was studied. In order to evaluate the system behaviour after large disturbances, the system response for DC fault on the line and single phase AC fault on the inverter side were simulated.

4.1. Step change in current reference

To simulate the response of the current command changes in an interval of time of 0.15 second for rectifier and inverter system, we should make the following steps:

At t = 0.6 s, a 20% step is applied on the reference current (decrease from 1 p.u. to 0.8 p.u.).

At t = 0.75 s, another step is applied to set the reference back to 1 p.u.

The figure 4 shows the response of the current regulator. The step change is effected in approximately 100 ms, and the step response is well controlled and stable.
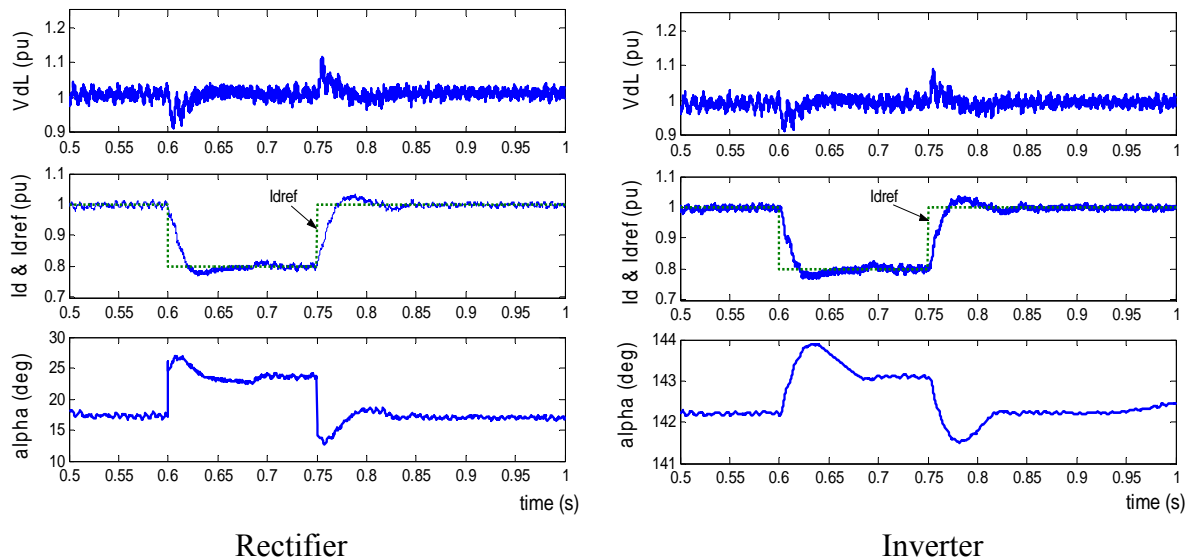

Rectifier   Inverter

Figure 4. Response to a 20% step of reference current

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4.2. DC Line fault

At fault application (t = 0.6 s), the DC current quickly increases to 2.3 p.u. and the DC voltage falls to zero at the rectifier. This DC voltages drop is seen by the Voltage Dependant Current Order Limiter (VDCOL), witch reduces the reference current to 0.3 p.u. at the rectifier (see figure 5). A DC current still continues to circulate in the fault. Then, at t = 0.65 s, the rectifier α firing angle is forced to 165 degrees. The rectifier now operates in inverter mode. The DC line voltage becomes negative and the energy stored in the line is returned to the AC network, causing rapid extinction of the fault current at its next zero-crossing. Then, α is released at t = 0.7 s and the normal DC voltage and current recover in approximately 0.5 s when the fault is cleared.

4.3. Single phase-ground fault at inverter

A single-phase-ground was applied to the A-phase of the inverter bus. The duration of the fault was 5 cycles. Results of this study are shown in figure 6. When this fault is applied at t = 0.6 s, due to a reduction in AC voltage of the inverter bus, the inverter DC voltage decreases. The DC current therefore shoots up. The rectifier current controller attempts to reduce the current by increasing its firing angle and the rectifier therefore goes into the inverter region. The DC current decreases to a low average value as determined by VDCOL. When the fault is cleared at t = 0.7 s, the VDCOL operates and rises the reference current to 1 p.u. The system recovers in approximately 0.3 s after fault clearing.
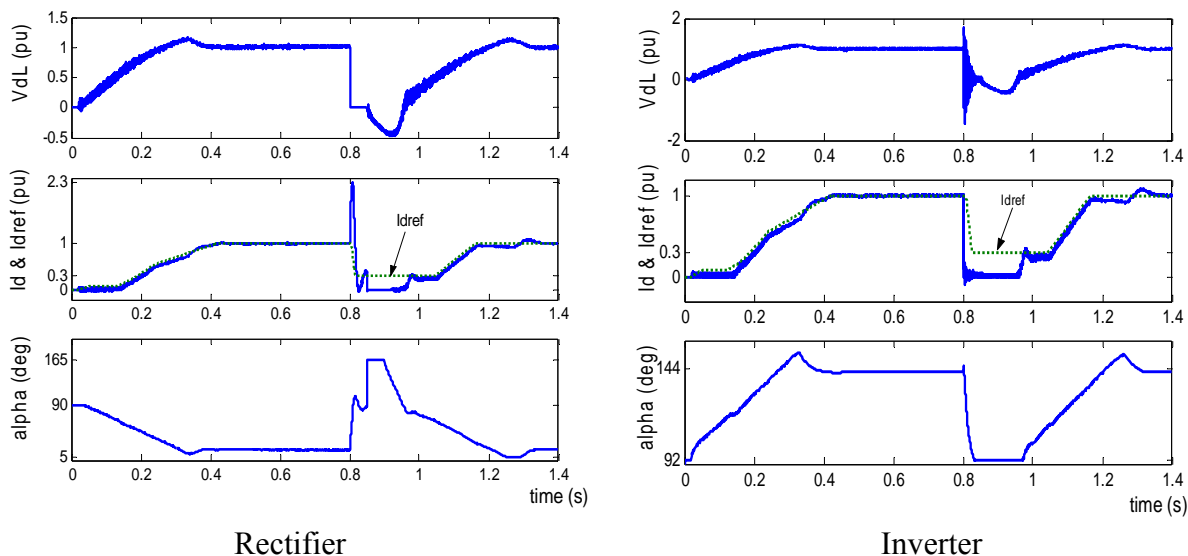

Rectifier   Inverter

Figure 5. DC line fault on the rectifier side

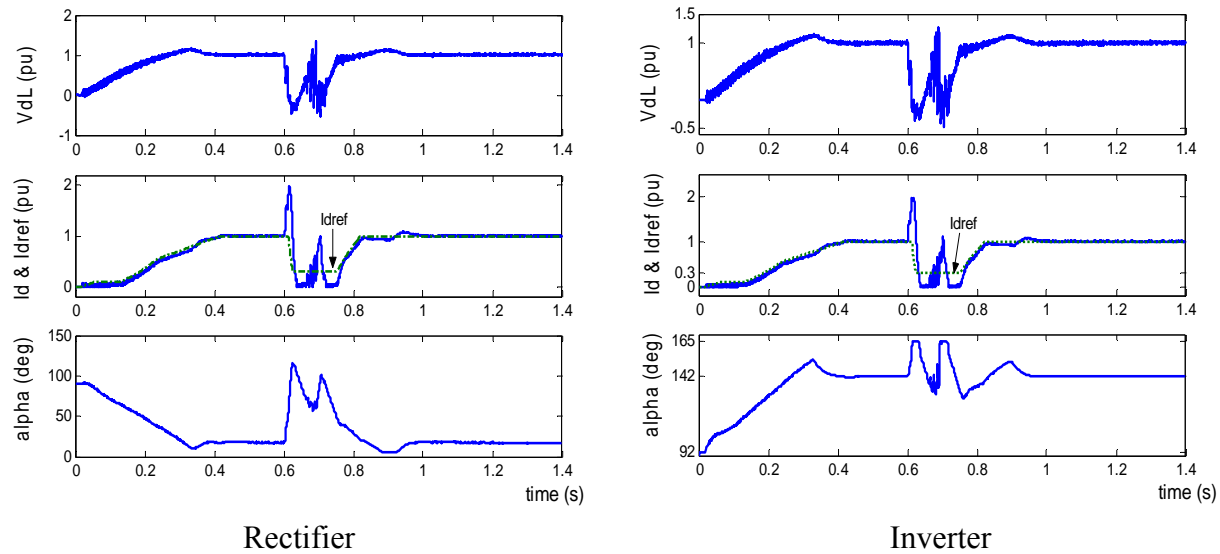Rectifier   Inverter

Figure 6. Single-phase-ground fault at inverter

5. CONCLUSION

Digital studies of transient disturbances were carried out using the Simulink in Matlab. Two cases are used to demonstrate the performance of the system.

From the results given above it can be seen that, in the case of DC fault, the voltage-dependent current order limits (VDCOL) function can have an important role in determining the DC system recovery from faults.

Faults on the inverter end leads to a reduction in the receiving end voltage. This causes an initial overshoot in the DC current. The system however recovers after the fault is cleared.

During normal operation, the rectifier is under current control mode and the inverter under extinction angle control mode. During faults, when the DC current reduces below the current reference of the inverter, the inverter takes control of current. After the fault is cleared, the current control is transferred back to rectifier.

If VDCOL function is activated during an inverter AC system fault, the result will be to decrease the DC current and hence the inverter reactive power consumption, thus helping to support the AC system voltage. In the case of severe single-line-to-ground faults, the VDCOL may also help to recover normal commutation, and thus some power transfer can resume during the fault. Following fault clearing, the removal VDCOL function current limit may be delayed and ramped so as to maximise the recovery rate, while avoiding subsequent commutation failures.

The results presented demonstrate the close agreement between the results of the system using Simulink and other simulation studies using EMTP and EMTDC [3, 6, 9].

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APPENDIX

Data for the system model:

Rectifier end:

The rectifier end AC system 1 (short circuit ratio = 5) consists of one source with an equivalent impedance of R = 26.07 Ω, L_1 = 48.86 mH, L_2 = 98.3 mH.

Inverter end:

The inverter end AC system 2 (short circuit ratio = 10) consists of one source with an equivalent impedance of R = 6.205 Ω, L_1 = 13.96 mH, L_2 = 28 mH.

DC line parameters:

R_{dc} = 0.015 Ω/Km, L = 0.792 mH/km, C = 14.4 nF/km.

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